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developed to design SoC on a heterogeneous FPGA CPU platform on the basis of performance metrics such as area, power, and latency. Design of physical downlink shared channel (PDSCH) in long term evolution (LTE) is presented as a case study. This paper provides the implementation of the transmitter

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## FPGA Implementation of Turbo Decoder for LTE Standard - CORE

Abstract This paper describes the implementation on field programmable gate array (FPGA) of a turbo decoder for 3GPP Long-Term Evolution standard. Considering the high data rates required by this standard, parallel decoding architecture is used.

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